FIG. 1A

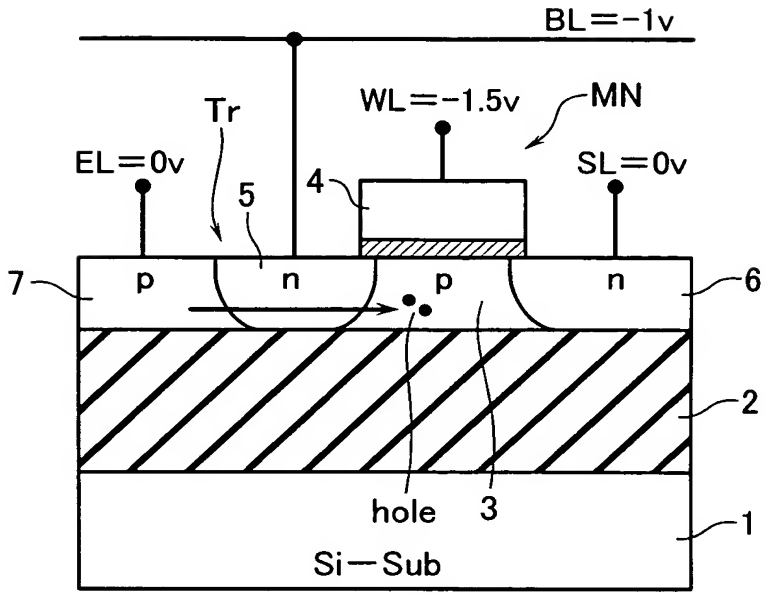

BL=-1v
WL=-1.5v
MN
Tr
EL=0v
SL=0v
4
5
7
p
n
p
n
6
2
hole
3
1
Si-Sub

FIG. 1B

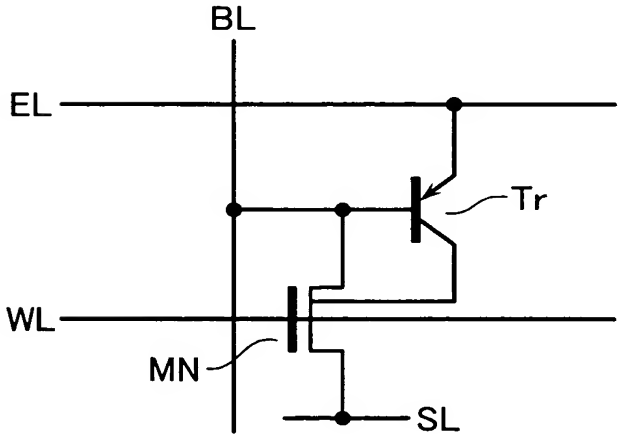

BL
EL
Tr
WL
MN
SL

FIG. 2

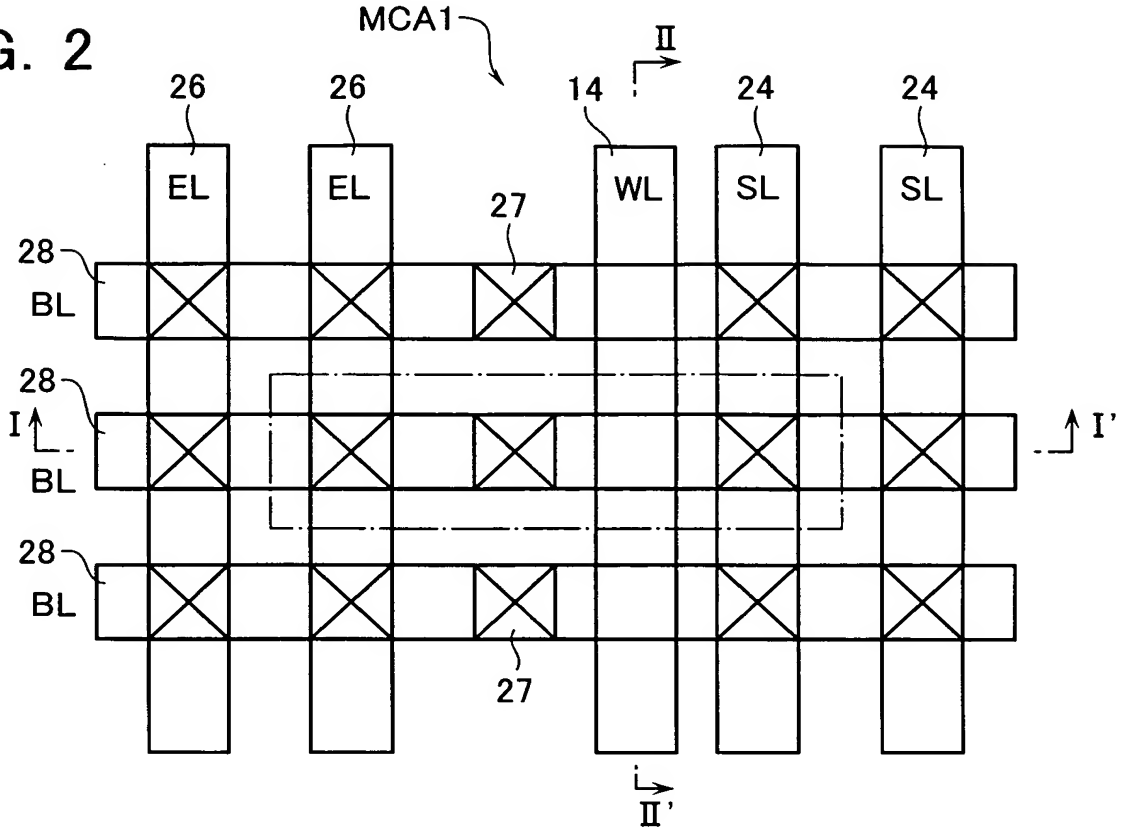

MCA1
II
26
26
14
24
24
EL
EL
27
WL
SL
SL
28
BL
28
I
I'
BL
28
BL
27
II'

FIG. 3

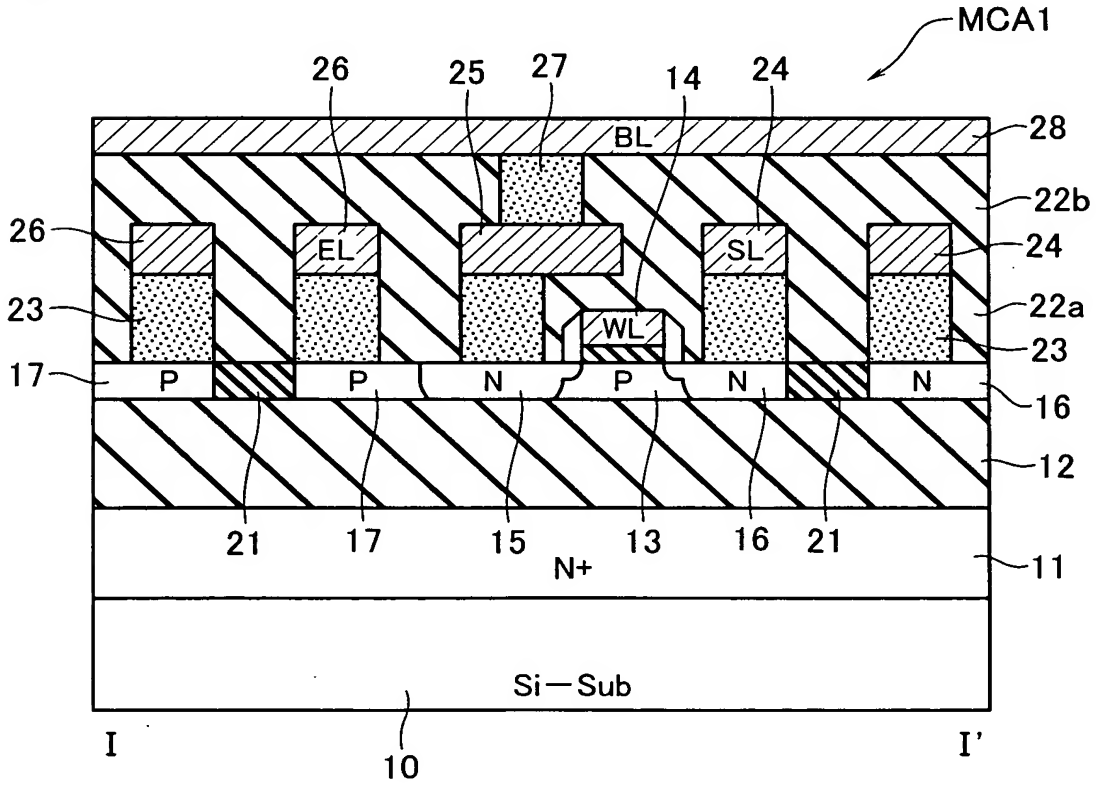

MCA1
26
25
27
14
24
28
BL
22b
26
EL
SL
24
23
WL
22a
23
17
P
P
N
P
N
N
16
12
21
17
15
13
16
21
11
N+
Si—Sub
I
10
I'

FIG. 4

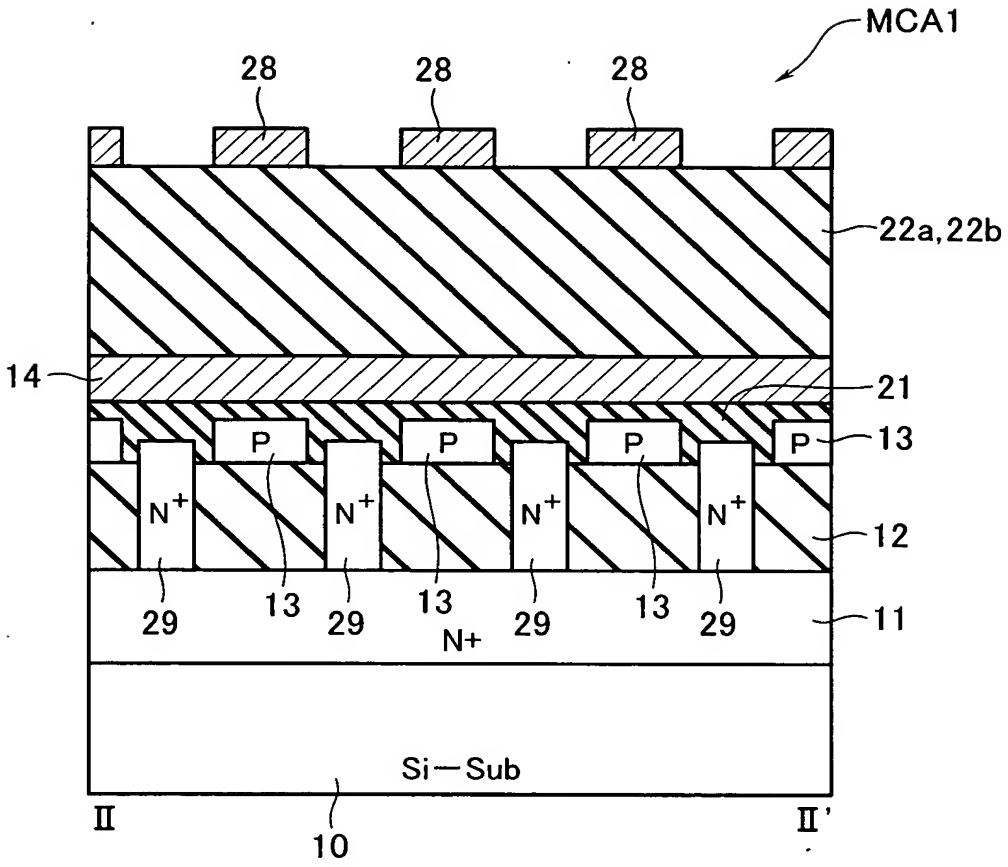

MCA1
28
28
28
22a,22b
14
21
P
P
P
P
13
N+
N+
N+
N+
12
29
13
29
13
29
13
29
N+
11
Si—Sub
II
10
II'

FIG. 5

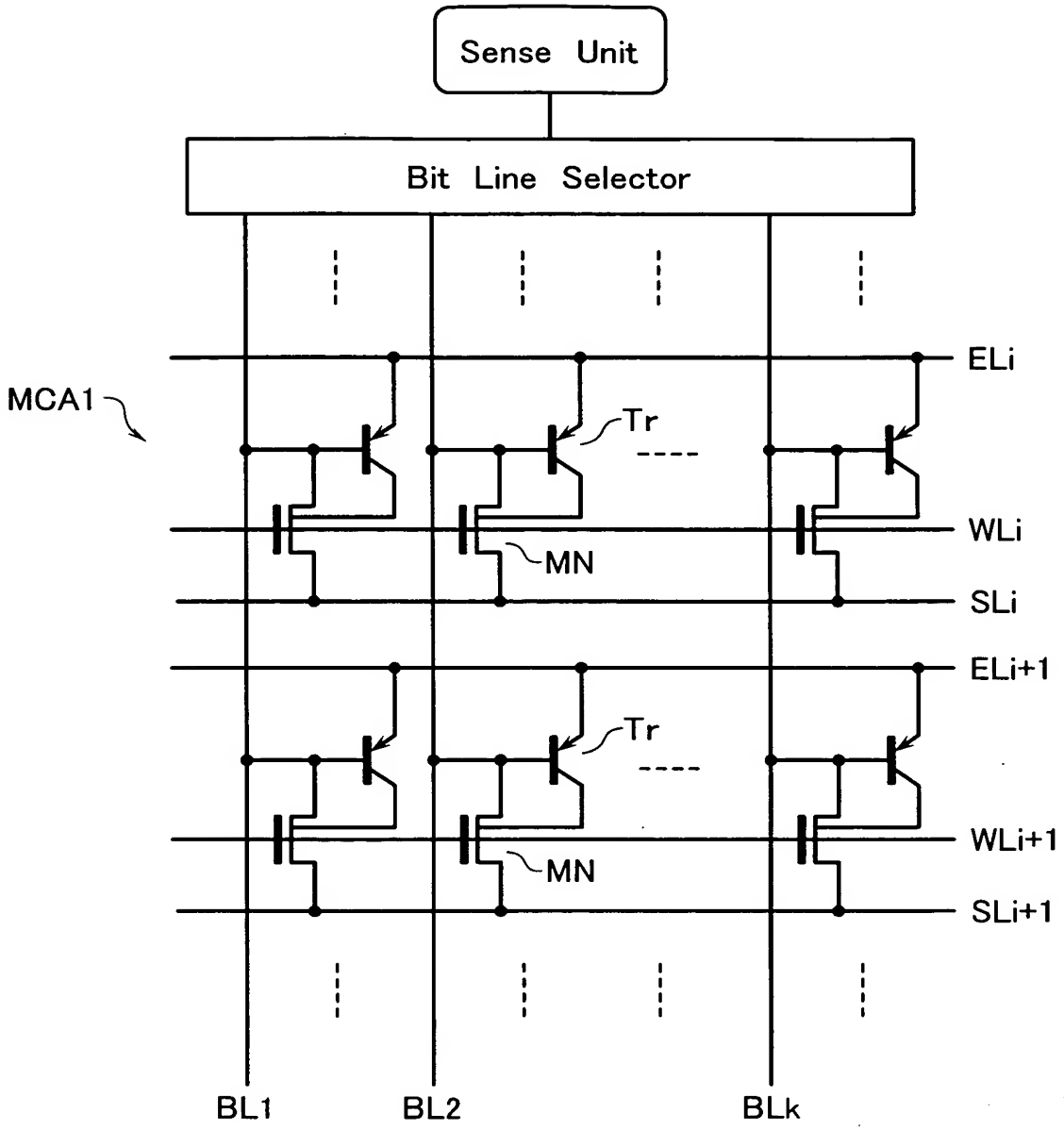

Sense Unit
Bit Line Selector
MCA1
ELi
Tr
WLi
MN
SLi
ELi+1
Tr
WLi+1
MN
SLi+1
BL1
BL2
BLk

FIG. 6

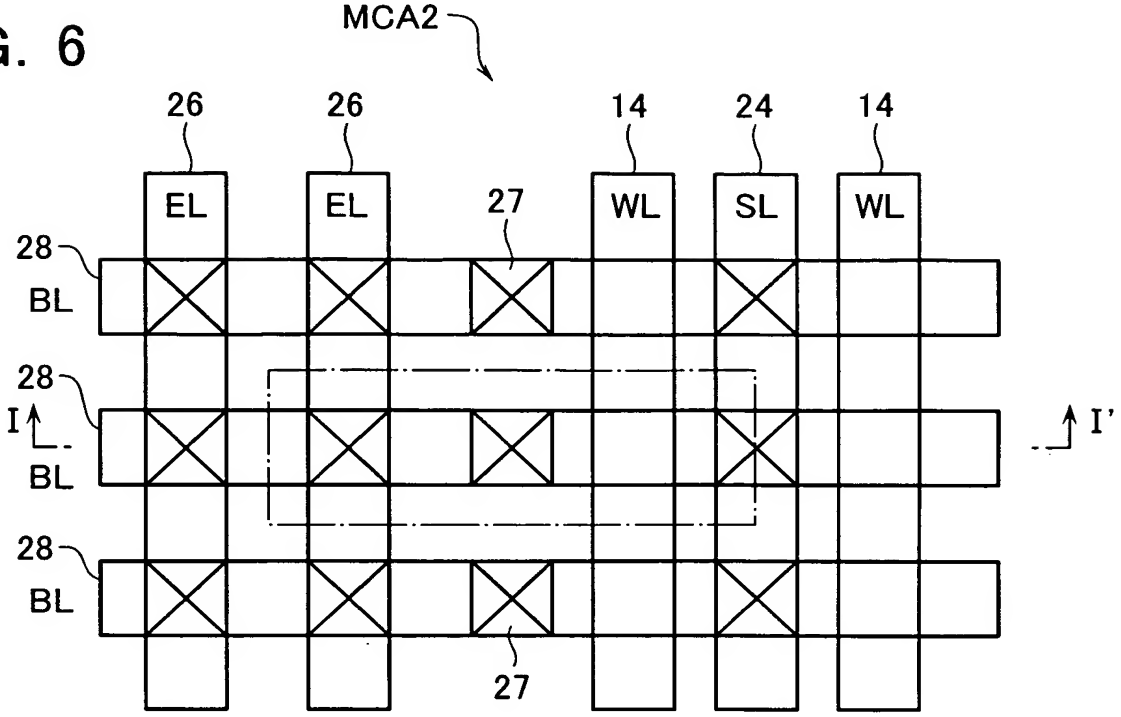

MCA2
26
26
14
24
14
EL
EL
27
WL
SL
WL
28
BL
28
BL
I
I'
28
BL
27

FIG. 7

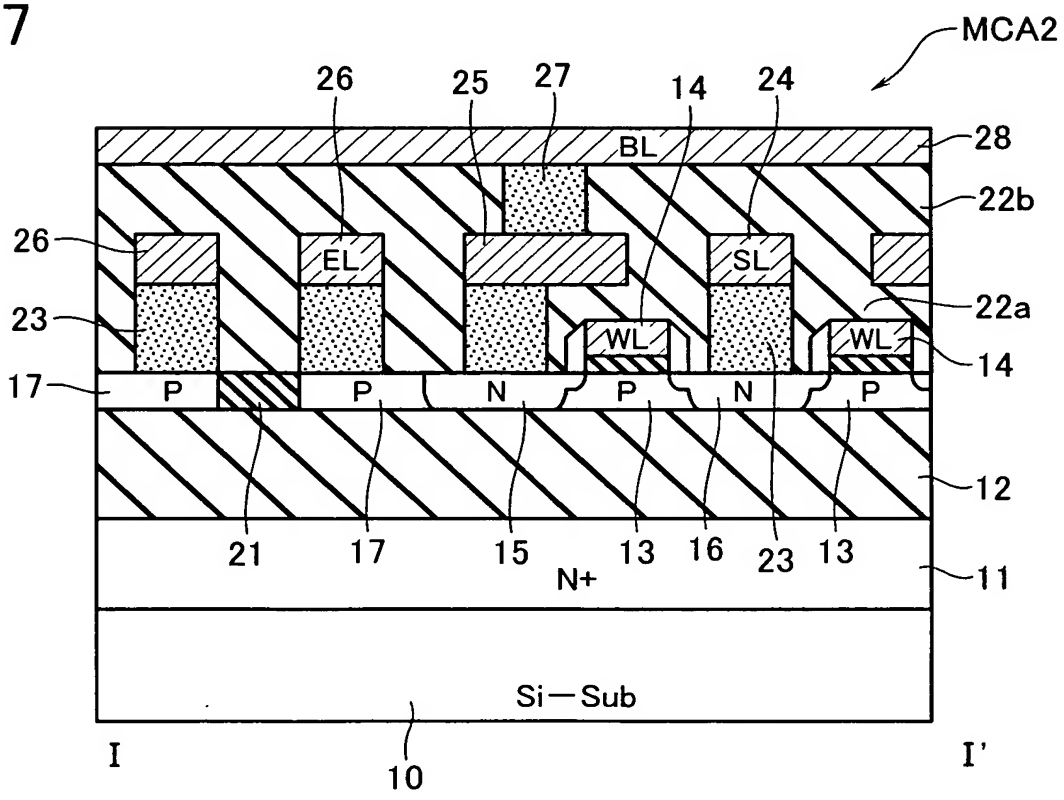

MCA2
26
25
27
14
24
BL
28
22b
26
EL
SL
23
22a
WL
WL
14
17
P
P
N
P
N
P
12
21
17
15
13
16
23
13
N+
11
Si—Sub
I
10
I'

FIG. 8

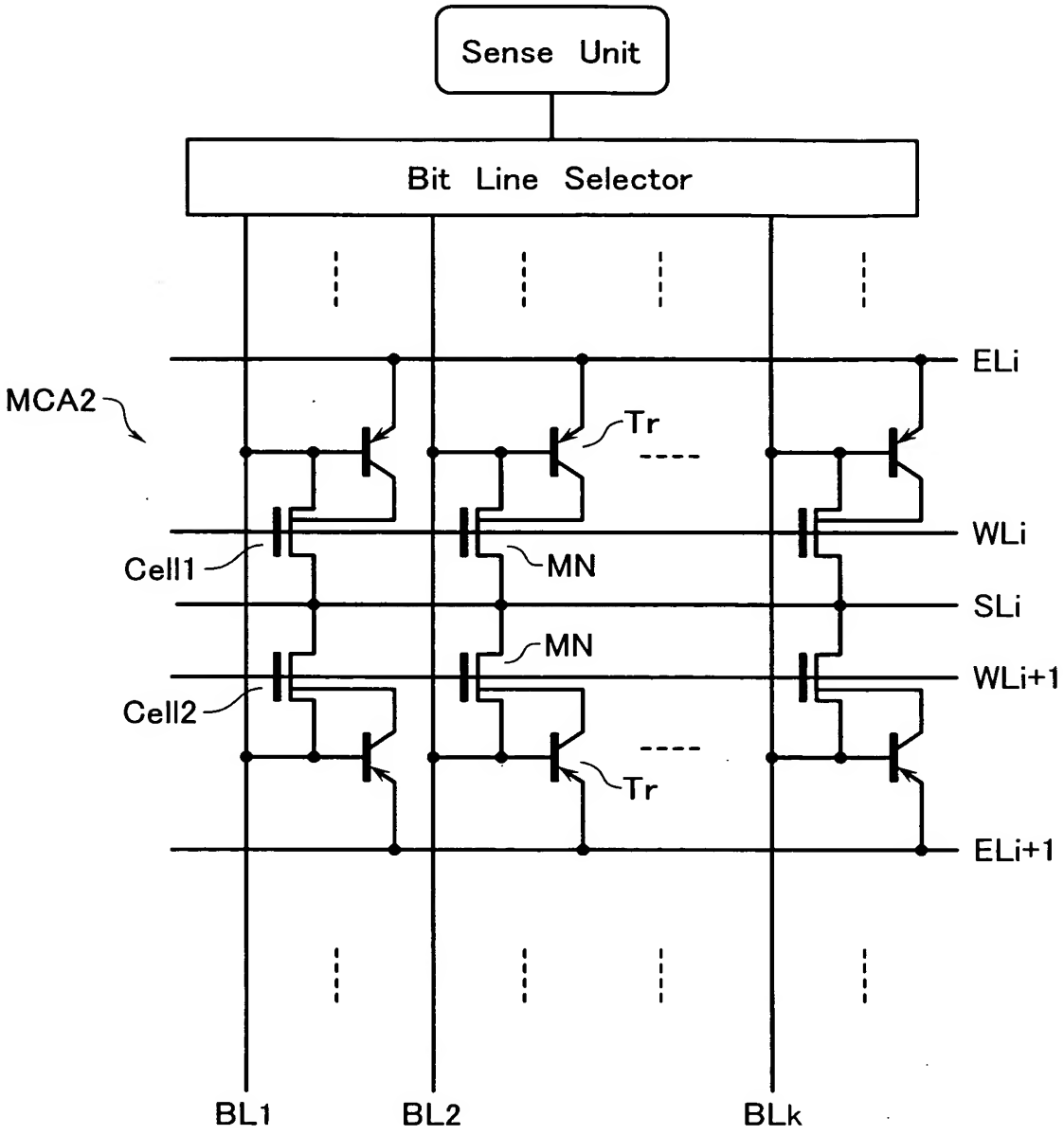

Sense Unit
Bit Line Selector
MCA2
Tr
ELi
WLi
Cell1
MN
SLi
MN
WLi+1
Cell2
Tr
ELi+1
BL1
BL2
BLk

FIG. 9

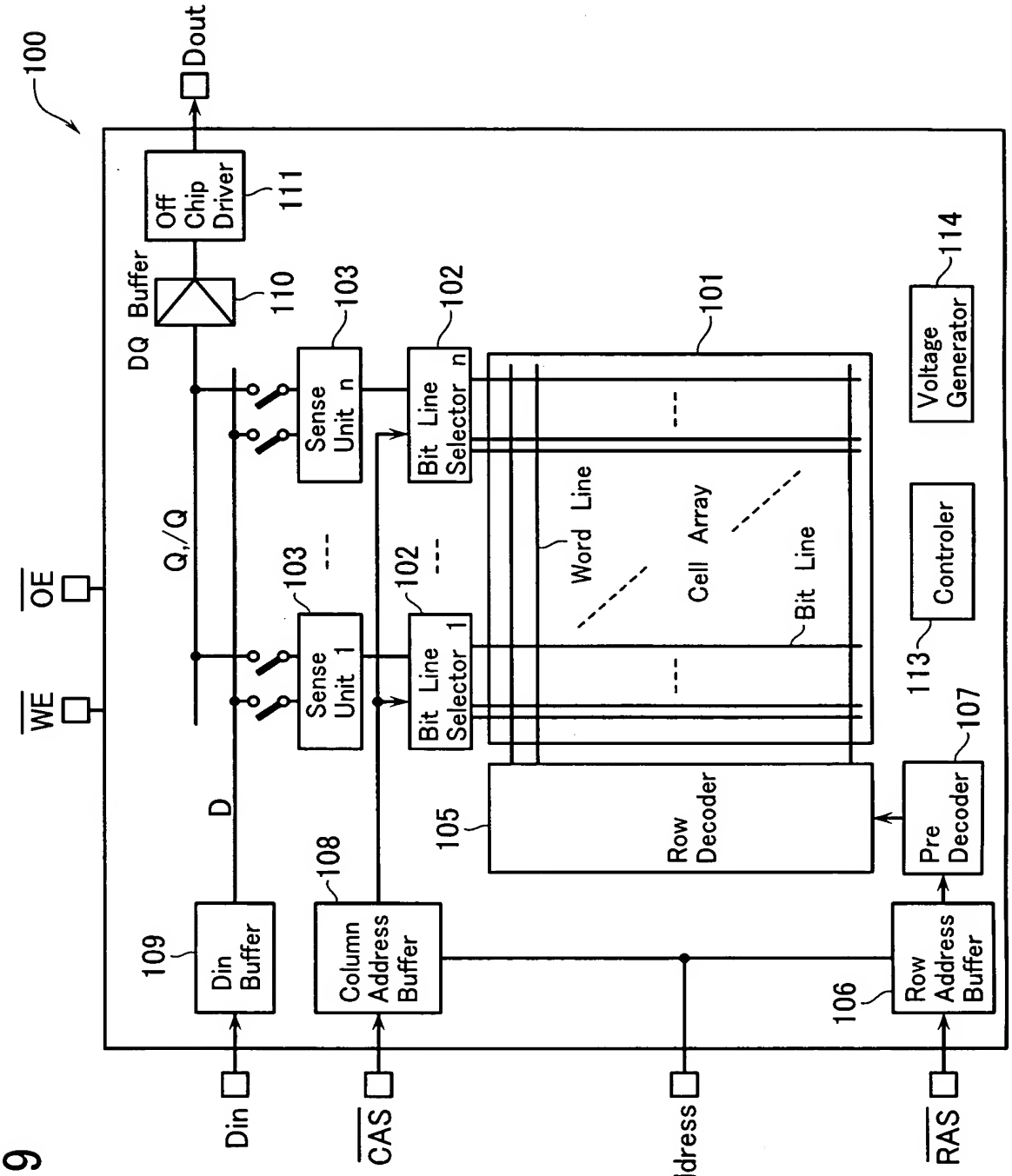

100
Dout
Off Chip Driver
111
DQ Buffer
110
103
102
101
114
Voltage Generator
Sense Unit n
Bit Line Selector n
Word Line
Cell Array
Bit Line
Controler
113
Q,/Q
OE
WE
Sense Unit 1
Bit Line Selector 1
107
Pre Decoder
105
Row Decoder
D
108
109
Din Buffer
Column Address Buffer
106
Row Address Buffer
Din
CAS
Address
RAS

FIG. 10

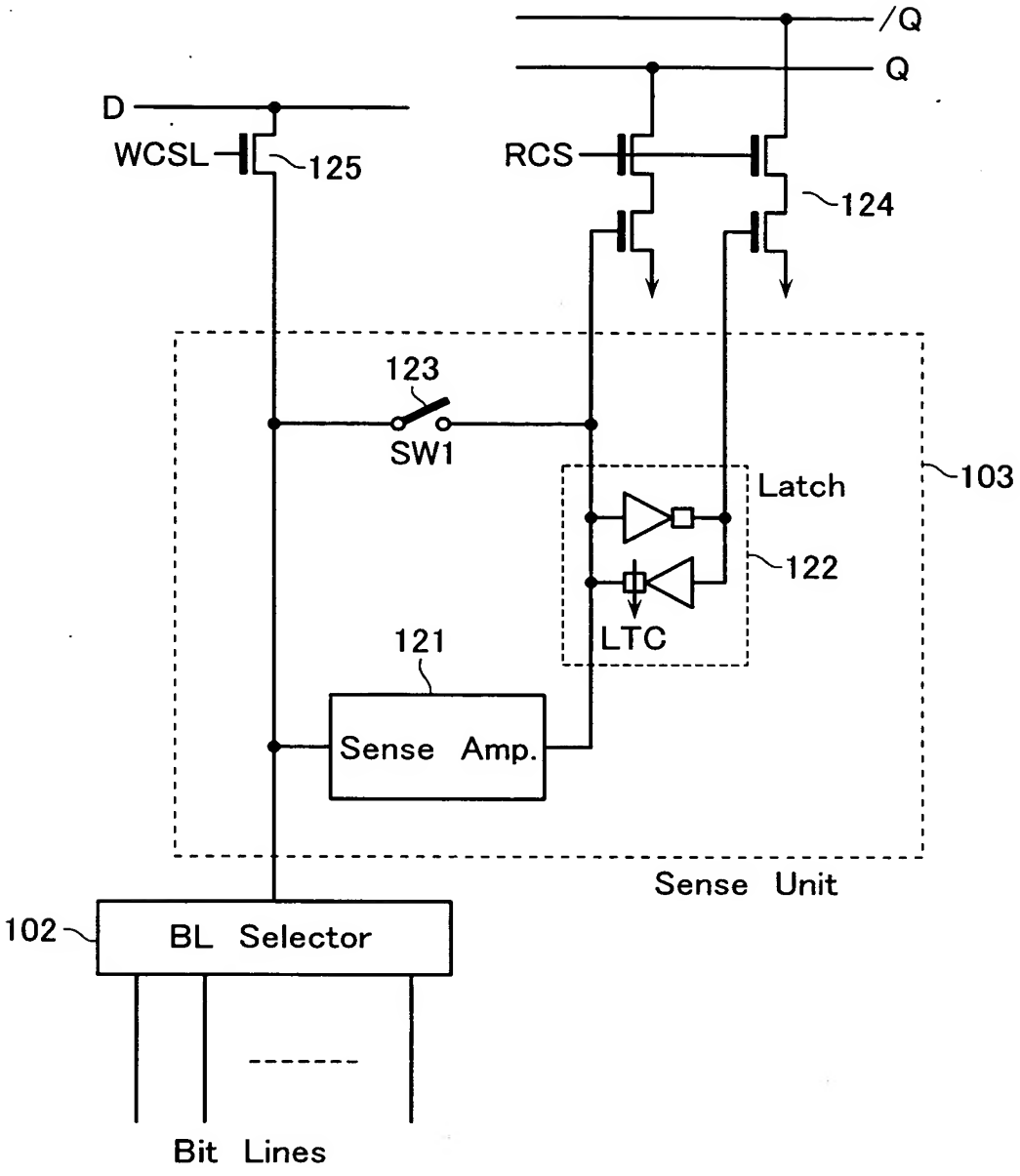

/Q
Q
D
WCSL
125
RCS
124
123
SW1
103
Latch
122
LTC
121
Sense Amp.
Sense Unit
102
BL Selector
Bit Lines

FIG. 11

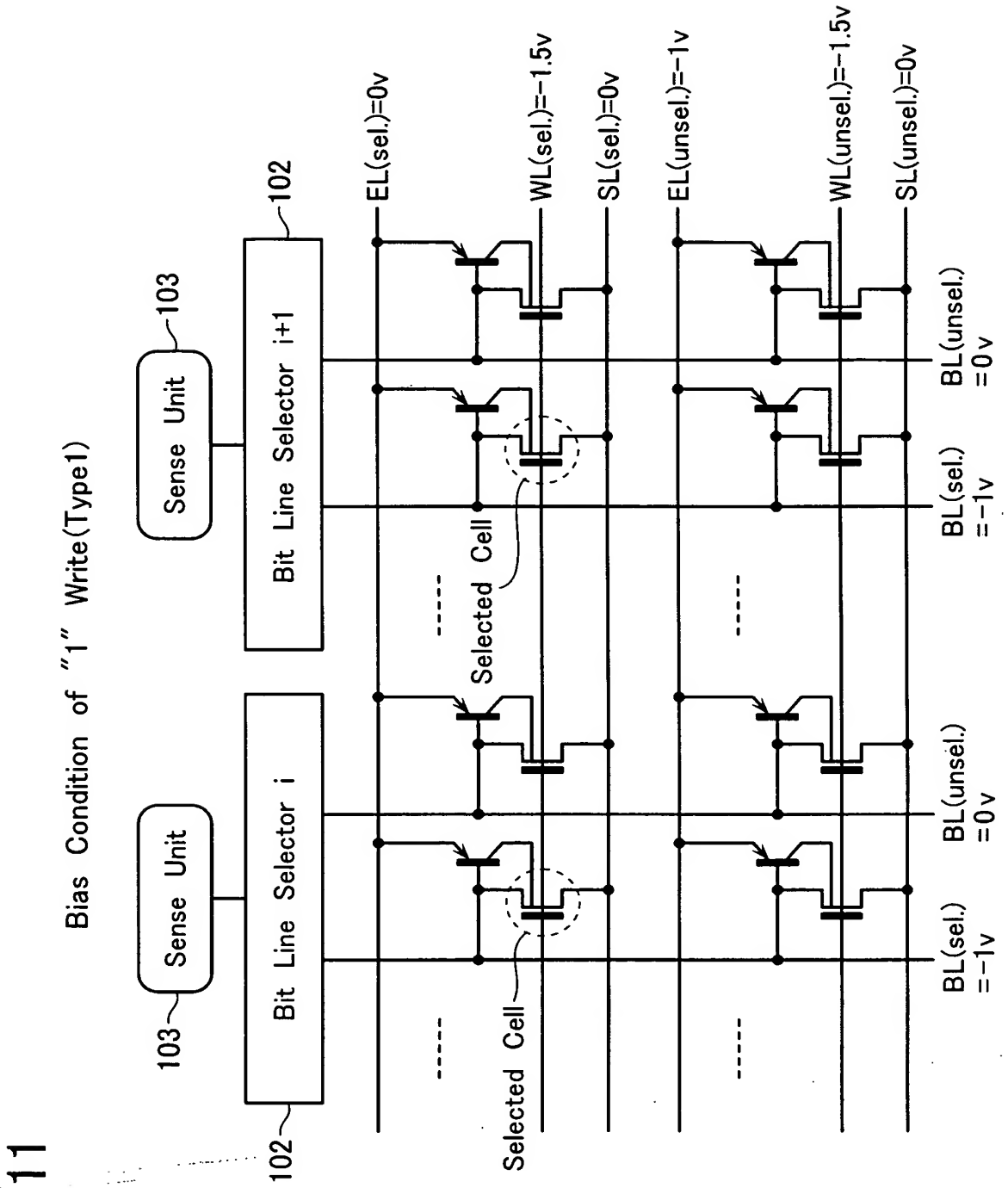

Bias Condition of "1" Write(Type1)
Sense Unit
103
Bit Line Selector i
102
Sense Unit
103
Bit Line Selector i+1
102
Selected Cell
Selected Cell
EL(sel.)=0v
WL(sel.)=-1.5v
SL(sel.)=0v
EL(unsel.)=-1v
WL(unsel.)=-1.5v
SL(unsel.)=0v
BL(sel.) =-1v
BL(unsel.) =0v
BL(sel.) =-1v
BL(unsel.) =0v

FIG. 12

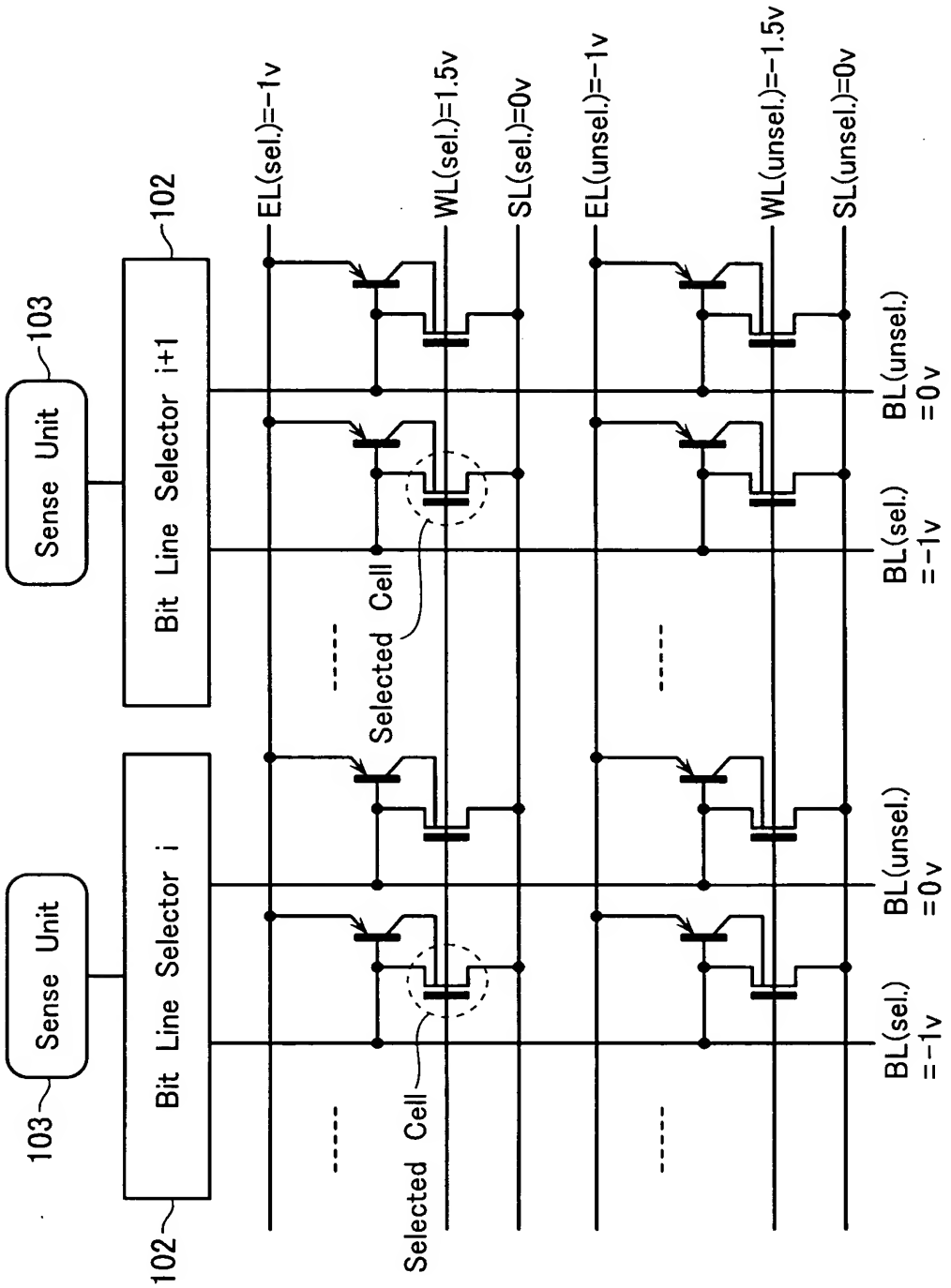

Bias Condition of "0" Write
Sense Unit
103
Bit Line Selector i
102
Sense Unit
103
Bit Line Selector i+1
102
EL(sel.)=-1v
WL(sel.)=1.5v
SL(sel.)=0v
EL(unsel.)=-1v
WL(unsel.)=-1.5v
SL(unsel.)=0v
Selected Cell
Selected Cell
BL(sel.) =-1v
BL(unsel.) =0v
BL(sel.) =-1v
BL(unsel.) =0v

FIG. 13

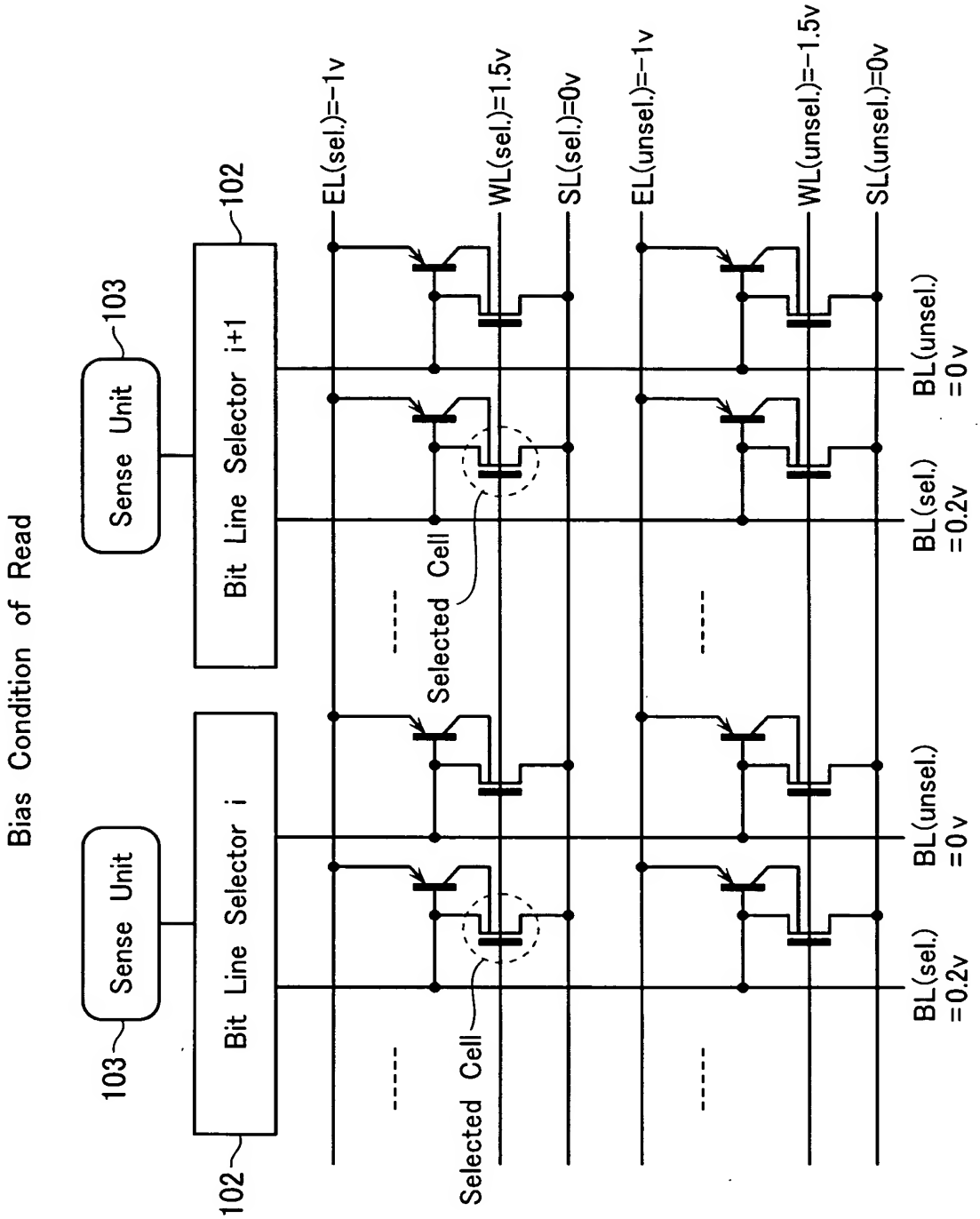

Bias Condition of Read
Sense Unit
103
Bit Line Selector i
102
Sense Unit
103
Bit Line Selector i+1
102
Selected Cell
Selected Cell
EL(sel.)=-1v
WL(sel.)=1.5v
SL(sel.)=0v
EL(unsel.)=-1v
WL(unsel.)=-1.5v
SL(unsel.)=0v
BL(sel.) =0.2v
BL(unsel.) =0v
BL(sel.) =0.2v
BL(unsel.) =0v

FIG. 14

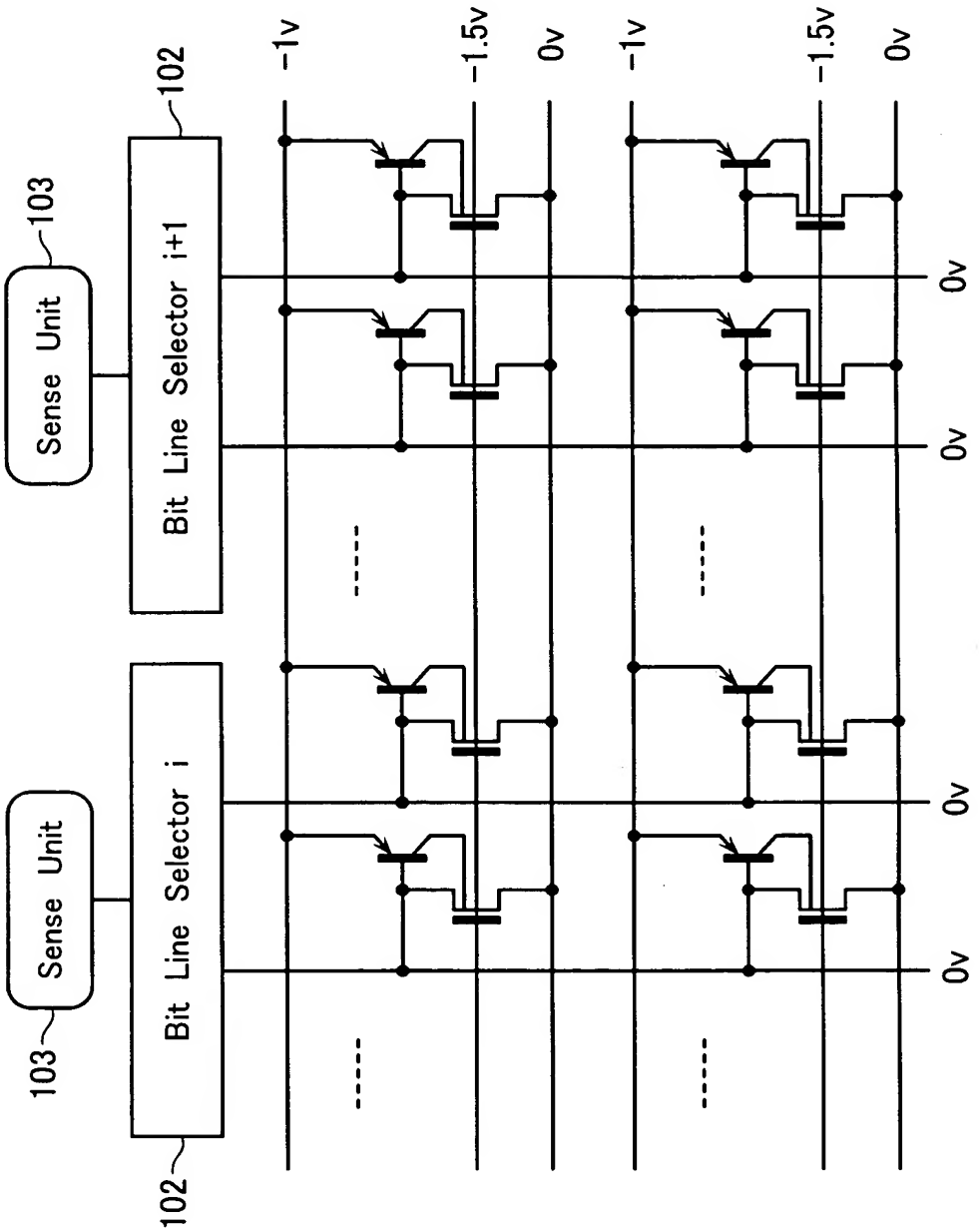

Bias Condition of Data Hold
Sense Unit
103
Bit Line Selector i
102
Sense Unit
103
Bit Line Selector i+1
102
-1v
-1.5v
0v
-1v
-1.5v
0v
0v
0v
0v
0v

FIG. 15

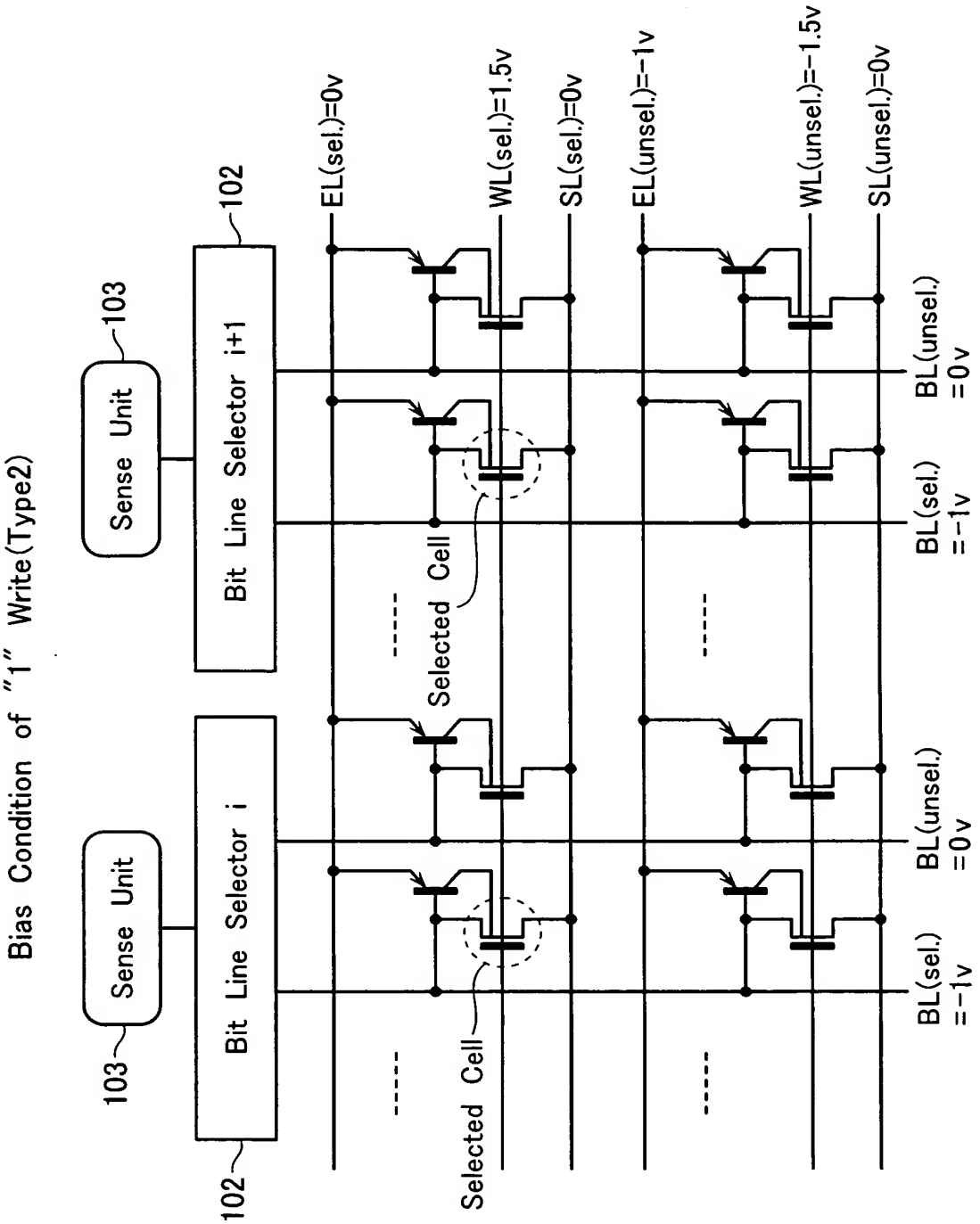

Bias Condition of "1" Write(Type2)
Sense Unit
103
Bit Line Selector i
102
Sense Unit
103
Bit Line Selector i+1
102
Selected Cell
Selected Cell
EL(sel.)=0v
WL(sel.)=1.5v
SL(sel.)=0v
EL(unsel.)=-1v
WL(unsel.)=-1.5v
SL(unsel.)=0v
BL(sel.) =-1v
BL(unsel.) =0v
BL(sel.) =-1v
BL(unsel.) =0v

FIG. 16

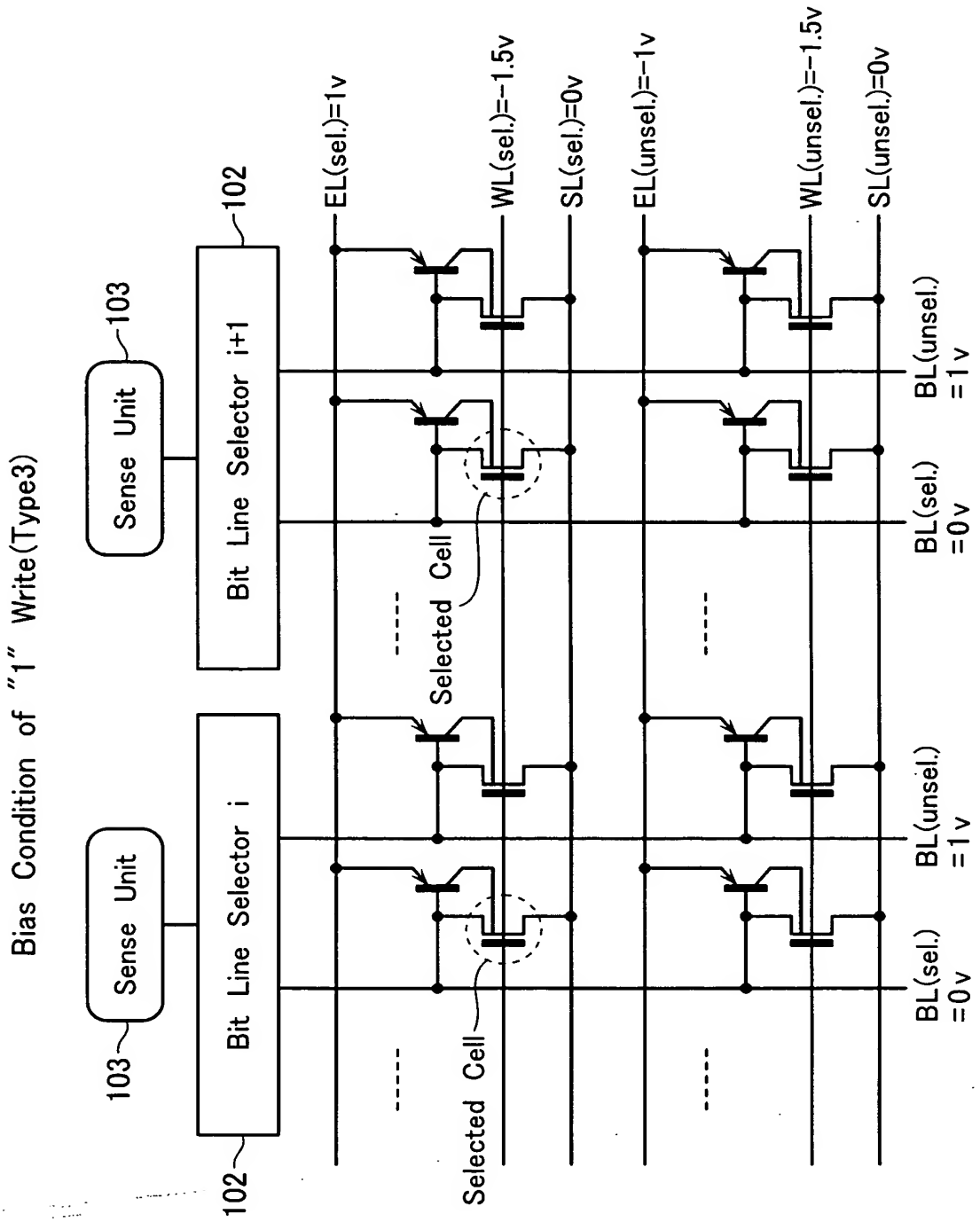

Bias Condition of "1" Write(Type3)
Sense Unit
103
Bit Line Selector i
102
Sense Unit
103
Bit Line Selector i+1
102
EL(sel.)=1v
WL(sel.)=-1.5v
SL(sel.)=0v
EL(unsel.)=-1v
WL(unsel.)=-1.5v
SL(unsel.)=0v
Selected Cell
Selected Cell
BL(sel.) =0v
BL(unsel.) =1v
BL(sel.) =0v
BL(unsel.) =1v

FIG. 17

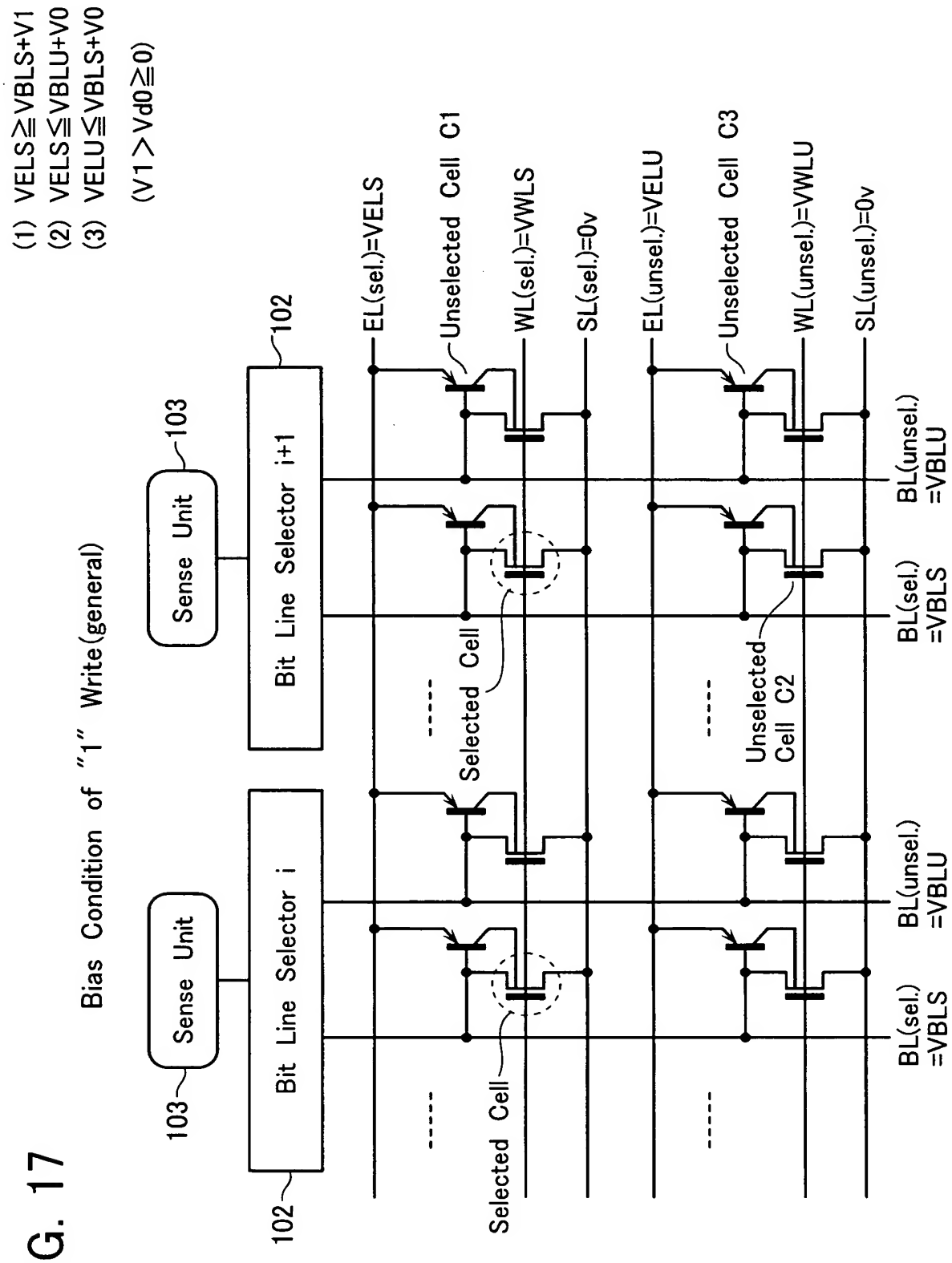

Bias Condition of "1" Write(general)
(1) VELS≧VBLS+V1
(2) VELS≦VBLU+V0
(3) VELU≦VBLS+V0
(V1 > Vd0≧0)
Sense Unit
103
Bit Line Selector i
102
Bit Line Selector i+1
102
Sense Unit
103
EL(sel.)=VELS
Unselected Cell C1
WL(sel.)=VWLS
SL(sel.)=0v
EL(unsel.)=VELU
Unselected Cell C3
WL(unsel.)=VWLU
SL(unsel.)=0v
Selected Cell
Selected Cell
Unselected Cell C2
BL(sel.) =VBLS
BL(unsel.) =VBLU
BL(sel.) =VBLS
BL(unsel.) =VBLU

FIG. 18

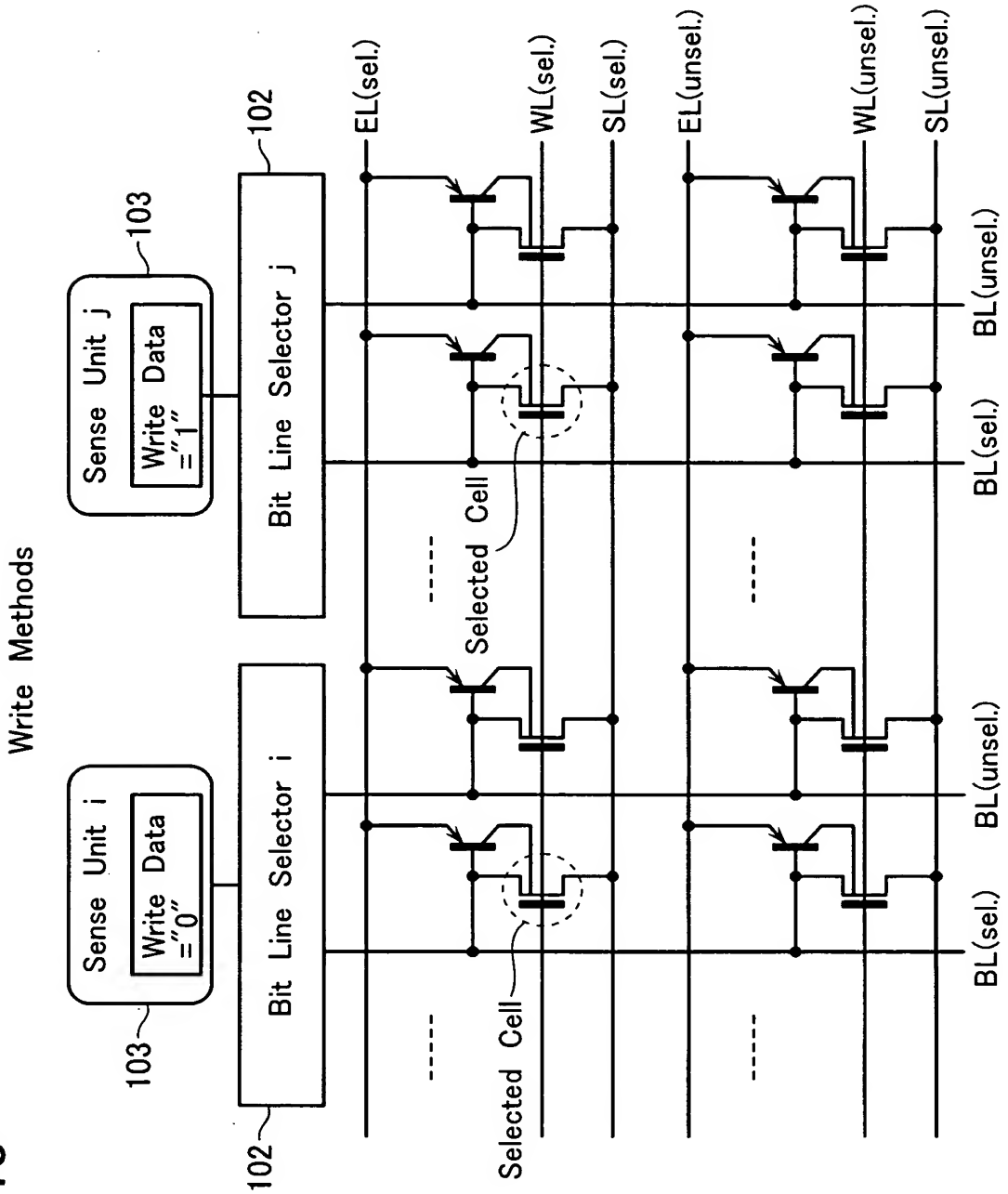

Write Methods
Sense Unit i
Write Data ="0"
Sense Unit j
Write Data ="1"
103
102
Bit Line Selector i
Bit Line Selector j
EL(sel.)
WL(sel.)
SL(sel.)
EL(unsel.)
WL(unsel.)
SL(unsel.)
Selected Cell
Selected Cell
BL(sel.)
BL(unsel.)
BL(sel.)
BL(unsel.)

FIG. 19

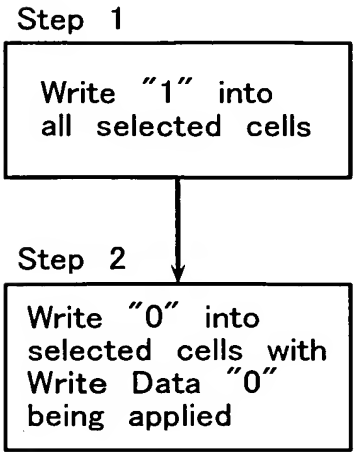


FIG. 20

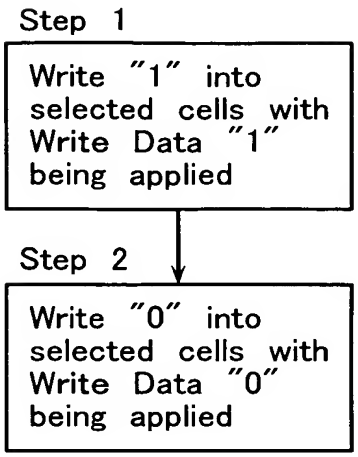


FIG. 21

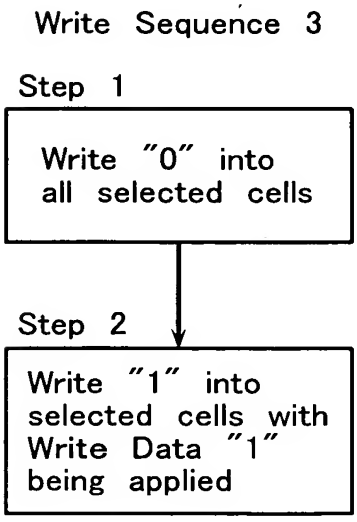


FIG. 22

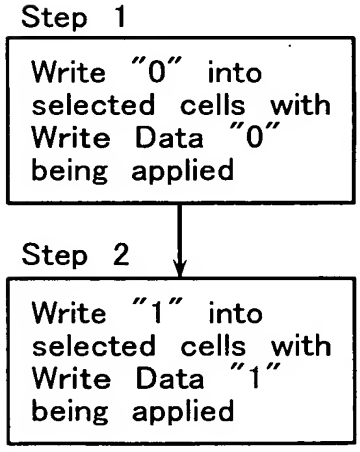


FIG. 23

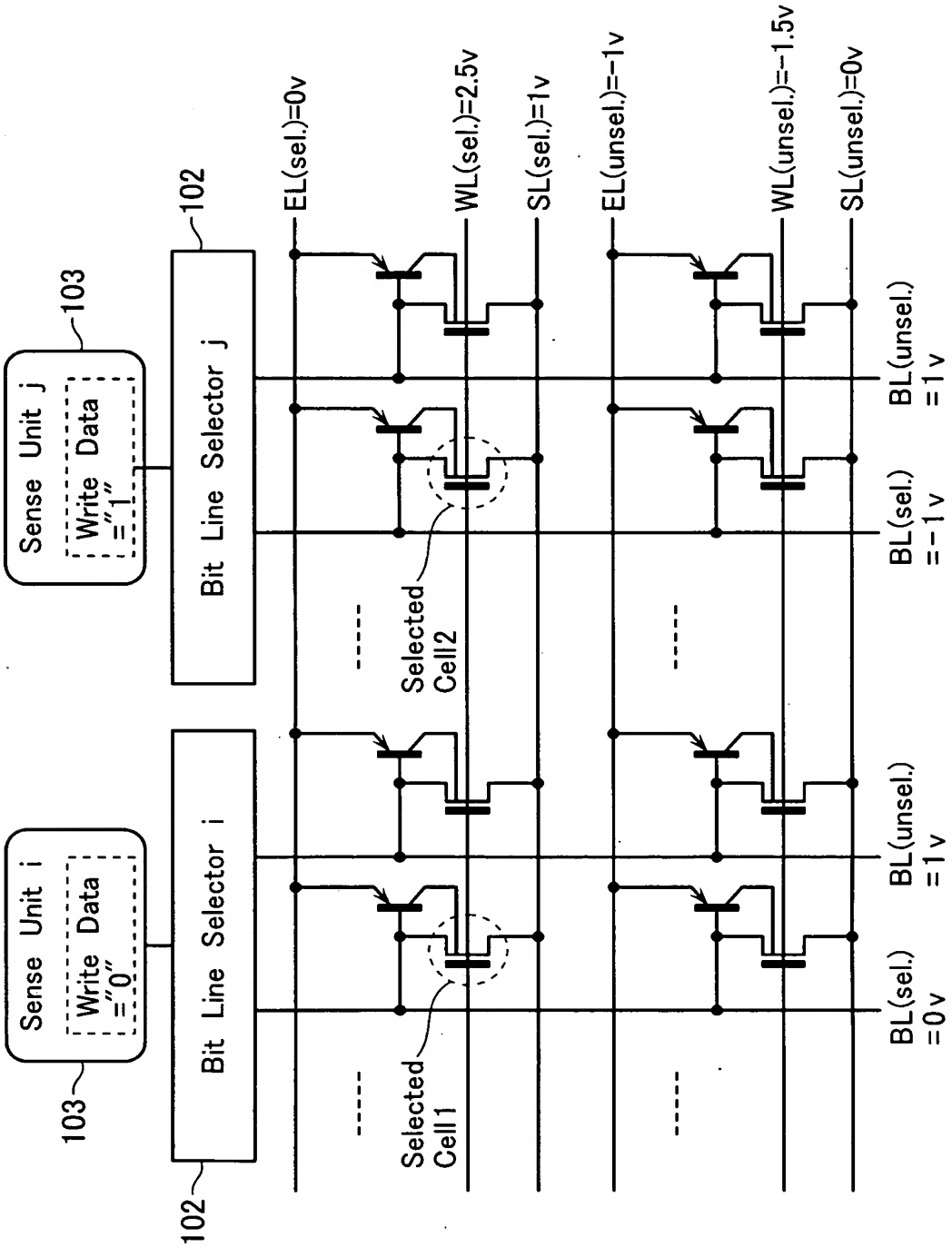
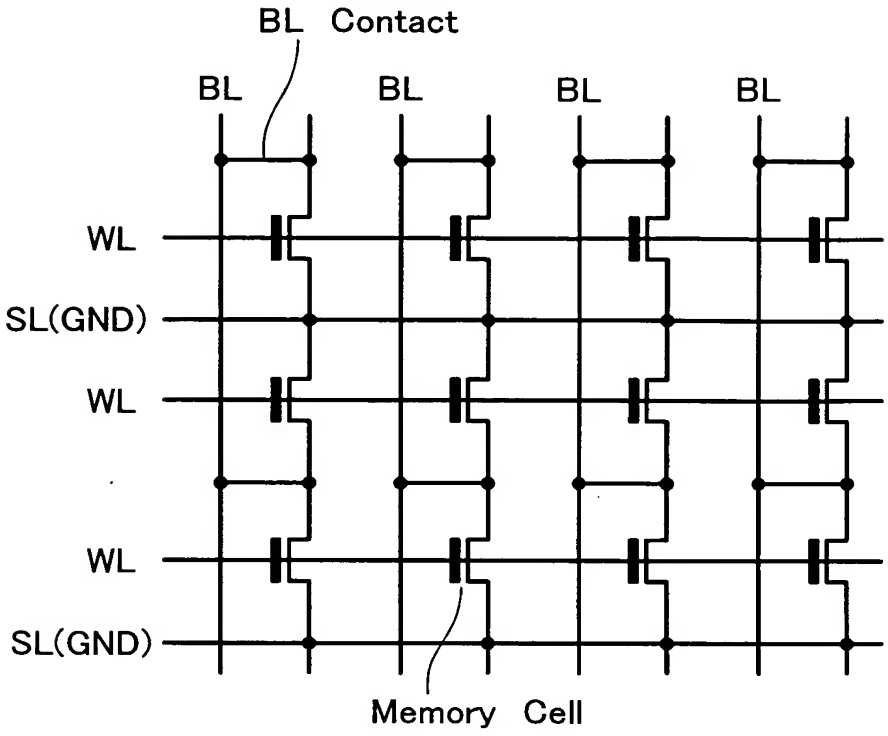
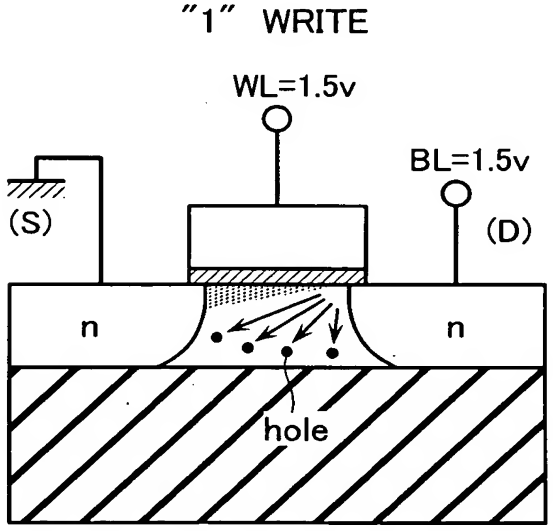

Sense Unit i
Write Data
="0"
Sense Unit j
Write Data
="1"
103
103
Bit Line Selector i
Bit Line Selector j
102
102
EL(sel.)=0v
WL(sel.)=2.5v
SL(sel.)=1v
EL(unsel.)=-1v
WL(unsel.)=-1.5v
SL(unsel.)=0v
Selected Cell1
Selected Cell2
BL(sel.) =0v
BL(unsel.) =1v
BL(sel.) =-1v
BL(unsel.) =1v

FIG. 24



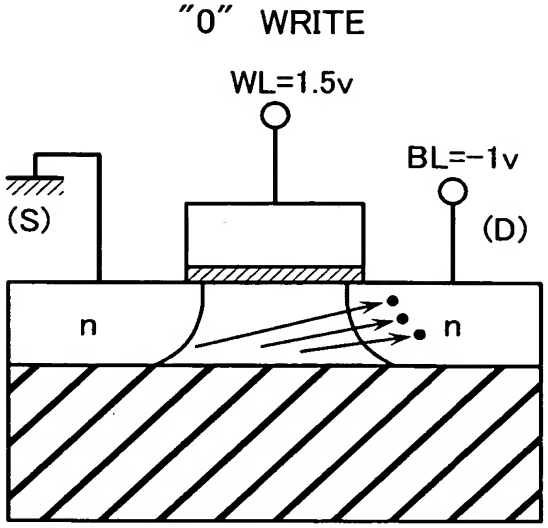
[PRIOR ART]

FIG. 25



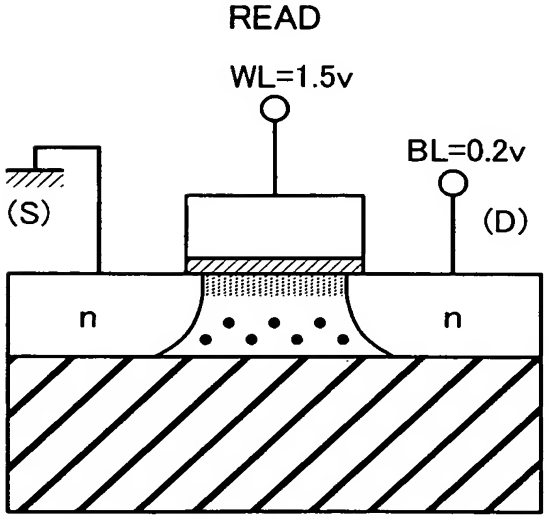
[PRIOR ART]

FIG. 26



[PRIOR ART]

FIG. 27



[PRIOR ART]

FIG. 28

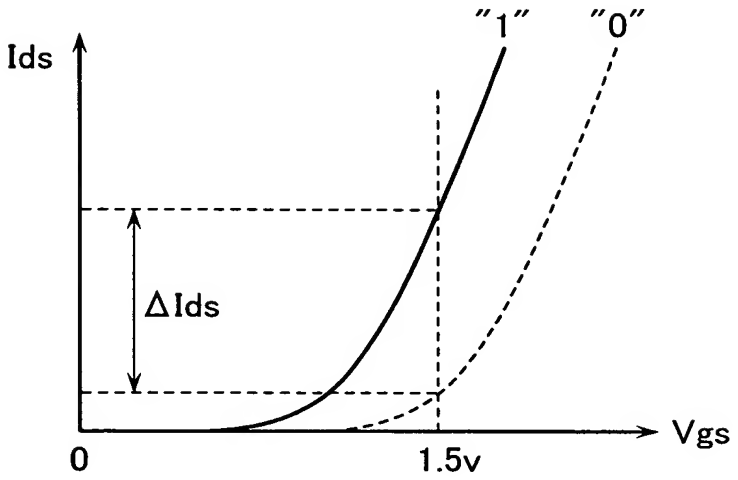
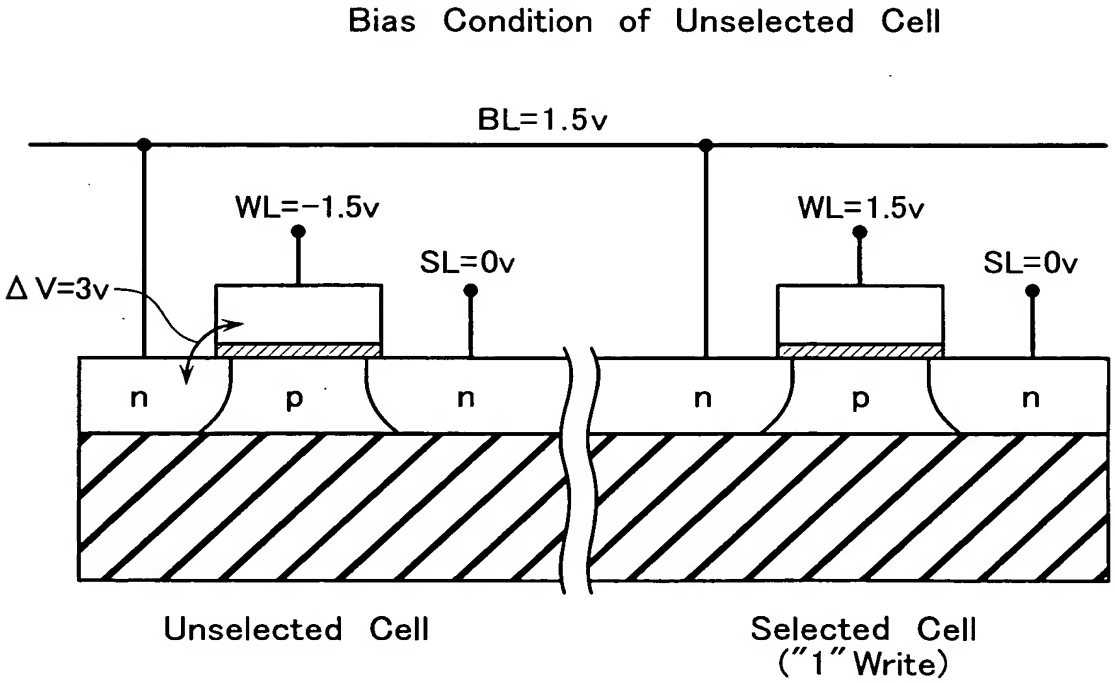


FIG. 29



[PRIOR ART]